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Boundary Layers Defect Diagnosis and Analysis of Through Silicon Via (TSV)

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Abstract

TSV technology can achieve heterogeneous integration by stacking different technologies and functions of logic chip, memory, MEMS, etc., as a system. There are many significant advantages for heterogeneous integration in terms of cost, performance, and time to market. TSV technology has the potential to improve 3D packaging. As the important physical connection and electrical connection between the chips, TSV's reliability is undoubtedly the key to determine the reliability of TSV three-dimensional integrated devices. As a new interconnect technology, TSV technology faces many process difficulties and challenges. Its reliability has not been fully studied and guaranteed. The process optimization and reliability improvement of TSV have become a hot topic in recent years. Recognition process defects and analysis of the failure mechanism play important roles in the optimization and improvement of design, production, and use of TSV three-dimensional integrated devices. In this paper, the square TSV and circular TSV with different ratios were researched by microphysical analysis and data analysis. The analysis results revealed the key technological factors and physical mechanism of formation of the TSV defects, which can support TSV device development, production, and reliable application.

Keywords: TSV; boundary layers; defect; failure analysis

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1. Introduction

With the development of 3D integrated packaging, through-silicon TSV has become one of the most promising technologies in 3D stacking packages [1-2]. Advanced TSV technology through the via and micro-bump achieves the vertical electrical connection between vertical stacks. It can also achieve the requirements of 3D heterogeneous integration of SiP, high-speed broadband, small size, and high performance.

TSV three-dimensional integrated devices with internal defects will gradually be failed by thermal mechanical stress, electrical stress, and other stresses, which will greatly affect TSV three-dimensional device reliability [3-4]. Ranganathan et al. [5] studied the influence of a fan-shaped interface generated by the Bosch etching process on TSV thermal stress. Koseski et al. [6] tested, modeled, and analyzed the stresses introduced by TSV with tungsten filling. Lau et al. [7] studied different spacing, different filling materials (copper and aluminum), and the thermal conductivity efficiency of different deep and wide ratio TSV chips. Chukwudi et al. [8] conducted a thermal cycling test on TSV and obtained the failure problems of void, crack, and oxidation in TSV under the condition of thermal cycling. Frank et al. [9] analyzed the reliability of TSV interconnecting for two technologies.

As a new interconnect technology, TSV technology faces many process difficulties and challenges [10-11]. The reliability has not been fully studied and guaranteed [12]. Identifying defects and analyzing the failure mechanism play important roles in the optimization and improvement of the design, production, and use of TSV 3D integrated devices [13-19].

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In this paper, the microscopic physical analysis of boundary layers of TSVs with different shapes and aspect ratios are carried out. The via drilling process quality and the uniformity of the boundary layers are evaluated. The physical mechanism of the formation of various process defects and the possible failure impact are analyzed. Finally, the corresponding improvement measures are put forward according to the failure reasons.

2. Through Silicon Via Technology

By making vias on the silicon wafer and filling conductive material inside, TSV technology achieves vertical conduction between the chip and chip combined with bumps. Compared with traditional gold wire bonding, the advantage of TSV is that it saves the three-dimensional volume occupied by the external conductor. TSV technology can make a microelectronics chip package achieve the most compact connection and the smallest three-dimensional size. In addition, due to a reduction in the length of the connection lines between the chips, the interconnect delay is greatly reduced, and thereby the operation speed is increased. Due to the reduction of the interconnect resistance, the circuit power consumption is also greatly reduced. TSV technology can achieve heterogeneous integration by stacking different technologies and functions of logic chip, memory, MEMS, etc., as a system. There are many significant advantages for heterogeneous integration in terms of cost, performance, and time to market. TSV technology has the potential to improve 3D packaging. In the mainstream device design and production process, TSV interconnect technology will become inevitable. TSV is recognized as a fourth-generation interconnect technology following wire bonding (WB), tape automated bonding (TAB), and flip-chip (FC). Figure 1 shows the development of electronic packaging in these four stages.

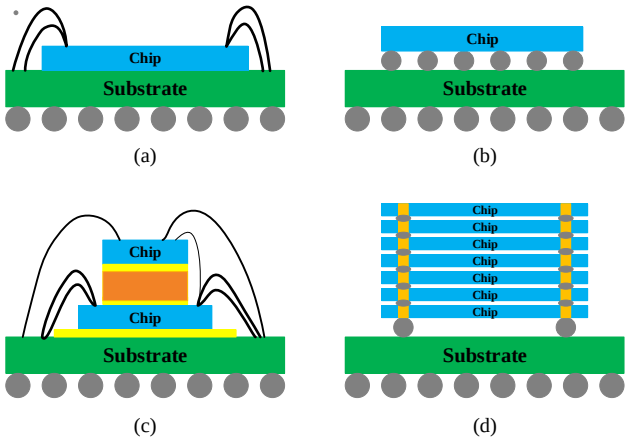


Figure 1. Electronic packaging development stages: (a) wire bonding circuit; (b) flip chip circuit; (c) wire bonding three-dimensional integrated circuit; (d) TSV three-dimensional integrated circuit

3. Typical Process Defects and Failure Mechanisms of TSV

3.1. Void

Void defects are mainly generated in the filling process of TSV. The filling voids of the metal may cause an increase in the TSV interconnect resistance, a change in the performance of the device, and even an open failure of the circuit.

Incomplete filling is the most common problem in TSV processes [20]. In the process of electroplating Cu, the plating current density plays a crucial role. According to previous studies, when the current density continues to increase, the Cu plating rate also increases. The copper-filled growth mechanism is grown from the sidewall to the middle. Therefore, with an increase in the current density, the rapid increase in the plating rate leads to the closing with copper at the opening of via and voids formation at the bottom of the via.

Due to the shelling effect caused in the etching process, the via wall is not flat and the wetting is bad, which is another key reason for the formation of TSV filling voids. Poor wetting of the via can also cause serious interceptive defects of the plated metal layer. Uneven deposition of the seed layer also creates voids.

In addition, bubbles at the bottom of the via prevent the bottom of the hole from filling completely. Therefore, an effective way to avoid voids is to take measures to remove the bubbles at the bottom of the via before plating. The vacuum pretreatment method can effectively improve the TSV electroplating effect, so that the copper filling rate can be close to 100%.

If the voids are located within the insulating layer along the sidewall of the TSV, this will result in shortage or leakage between the TSV and the substrate.

3.2. Protrusion

After plating copper, redundant copper on the wafer surface needs to be removed by chemical mechanical polishing (CMP). Then, annealing follows. Due to the mismatch of the coefficient of thermal expansion (CTE) between Cu and Si, great thermal-mechanical stress is generated in TSV by the large temperature change before and after annealing. Due to the constraint of the surrounding Si substrate, Cu can only vertically expand outward in order to release the internal stress, which is called protrusion [21]. High temperature annealing also can cause lattice defects because of grain growth, as shown in Figure 2.

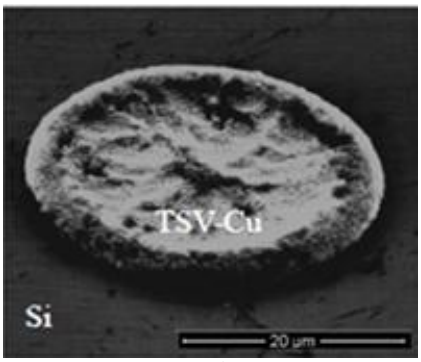


Figure 2. Protrusion morphology of TSV-Cu during thermal cycling

Protrusion occurs in the annealing process, so the protrusion is influenced by different annealing conditions. It is shown that the annealing temperature is an important influence factor for protrusion [22]. The higher the annealing temperature, the more obvious the protrusion. In addition, the annealing time and TSV diameter, depth, spacing, and other parameters also have a certain role on the formation of protrusion.

Protrusion is an expression form of stress release. It will impact the reliability of the TSV device. On the one hand, the circuit around TSV can be extruded to failure by protrusion of TSV-Cu [23]. On the other hand, the structure around TSV can be pulled by protrusion of TSV-Cu, which will cause the metal interconnect layer to break (e.g. BEOL layer) [24].

3.3. Fracture and Delamination

Fracture and delamination are other major defects of TSV devices under high temperature processes, as shown in Figure 3. At present, in the typical process of TSV manufacturing, the material filled with vias as the conductor is mainly copper. Since the CTE among the filled Cu, Si substrate and the SiO_2 insulating layer do not match with each other [25], significant thermo-mechanical stresses will be generated inside TSV in the manufacturing process. Under thermo-mechanical stress, TSV and micro-bumps may fracture, and micro-bumps may undergo delamination with TSV or bonding pads. Fracture and delamination may change the electrical properties of TSV devices, such as by increasing interconnection resistance.

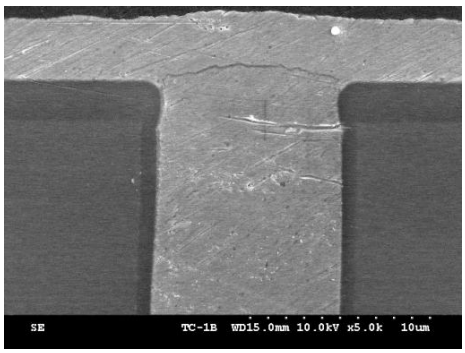


Figure 3. Propagation of crack along the Top-M1-TSV interface after thermal cycles

4. Experiment and Analysis

4.1. Sample Introduction

The TSV sample chip had a total of 24×20 vias. The left 12×20 vias were square. The right 12×20 vias were circular. The diameter or side length of each series of vias from left to right was decreased in turn, and it was always the same from top to bottom, as shown in Figure 4.

The first three process steps were completed including via drilling, isolation/buffer layer preparation, and Cu seed layer deposition. The boundary layers of the via are shown in Figure 5. Via filling, CMP, chip thinning, and bonding with other chips had not been completed.

The depths of all the vias were almost the same, about 110 ~ 120 μm. The diameter or side length ranged from 15 μm to 95 μm. And the aspect ratio (AR) ranged from 1:1 to 5:1.

A series of vias on the chip should be defined before the experiment. Square vias by side length from large to small were named S1, S2, S3, ⋯, S12. Circle vias by diameter from large to small were named C1, C2, C3, ⋯, C12.

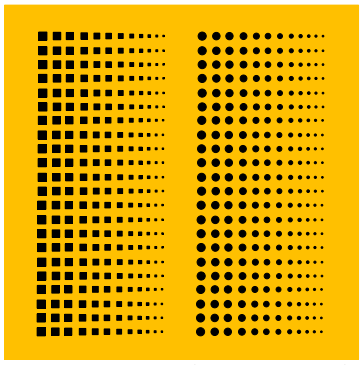


Figure 4. Appearance of TSV sample surface

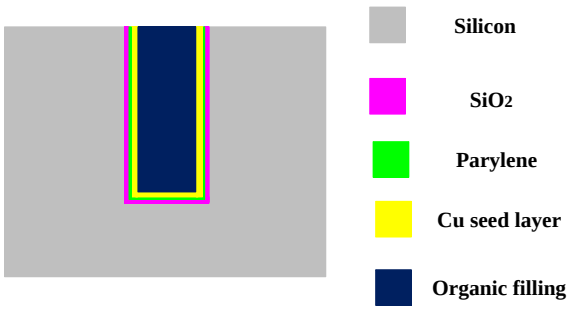


Figure 5. TSV sample boundary layer material schematic

4.2. Via Drilling Process Quality Analysis

To evaluate via drilling process quality, cross section analysis was performed on the sample. As shown in Figure 6, the series of silicon vias were narrow at the top and wide at the bottom.

Further analysis found that the larger the aspect ratio, the greater the difference between the top and bottom via diameter or side length, as shown in Figure 7. The red points represent the percentage of square vias side length difference between the top and the bottom. The green points represent the percentage of circle vias diameter difference between the top and the bottom. For the C12 silicon, the bottom via diameter was 27% more than the top.

Vias drilling of the sample was done using Bosch etching, a deep reaction-ion etching process that can form high aspect ratio features. By adjusting the ratio of the shielding gas C4F8 and the etching gas SF6, the shape of the vias could be changed. When the gases ratio was properly adjusted, vertical silicon vias were obtained, as shown in Figure 8(a). When the shielding gases ratio was larger, inverted trapezoidal silicon vias were obtained, as shown in Figure 8(b). When the etching

gases ratio was larger, positive trapezoidal silicon vias were obtained, as shown in Figure 8(c). When the shielding gases were not used, oval vias were obtained, as shown in Figure 8(d).

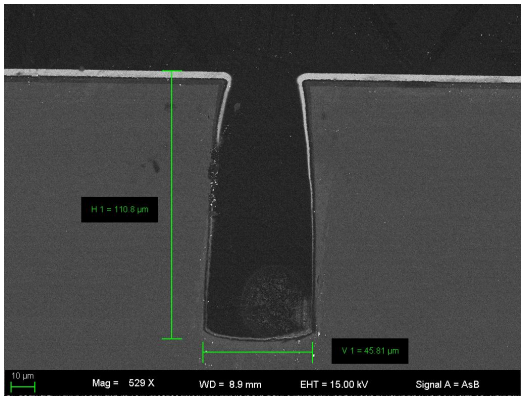


Figure 6. Typical via cross section

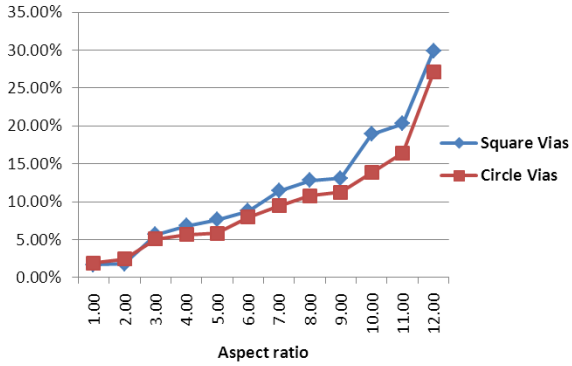


Figure 7. Curves of via diameter or side length difference between the top and the bottom with aspect ratio

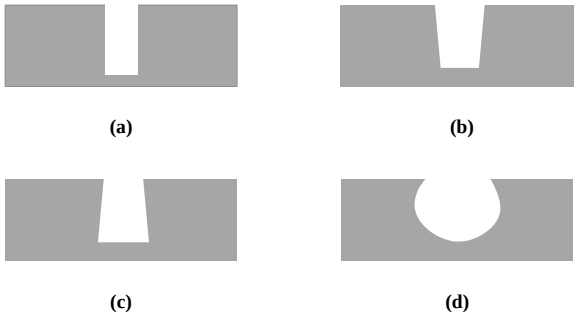


Figure 8. Silicon vias of various shapes: (a) vertical; (b) inverted trapezoidal; (c) positive trapezoidal; (d) oval

Obviously, the etching gases ratio was larger in the drilling process for this sample, so the vias were positive trapezoidal. These positive trapezoidal vias would cause the silicon via closing in advance at the top in the next filling process, so the silicon via could not be filled completely, as shown in Figure 9.

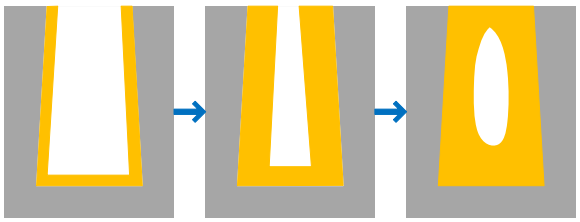


Figure 9. Silicon via closing in advance at the top

4.3. Boundary Layers Quality Analysis

In order to evaluate boundary layer quality, 15 measurement points were taken on the vias sidewall to measure the thickness for each boundary layer, as shown in Figure 10.

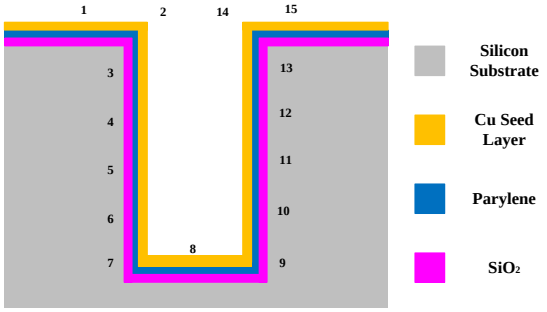


Figure 10. Measurement points for each boundary layer

As shown in Figure 10, there are several important points that need to be noted. The measurement point 1 and the measurement point 15 recorded the thickness of the boundary layers on the wafer surface. The measurement points 2 and 14 recorded the thickness of the boundary layers at the top corner. The measurement point 7 and the measurement point 9 recorded the thickness of the boundary layers at the bottom corner. The measurement point 8 recorded the thickness of the boundary layers in the center of the bottom. S3 was selected as an example, and it had a width of about 80 μm, depth of about 120 μm, and aspect ratio of 1.5:1. The specific data is shown in Table 1.

Table 1. Thickness data of the boundary layers of S3

Point	Cu seed layer (μm)	Parylene layer (μm)	SiO_2 layer (μm)
Point 1	2.89	1.13	2.30
Point 2	2.34	0.99	1.94
Point 3	1.56	0.85	1.18
Point 4	1.27	1.02	1.00
Point 5	0.47	0.99	0.39
Point 6	0.68	0.97	0.33
Point 7	0.80	0.76	0.36
Point 8	0.71	0.86	0.42
Point 9	1.11	0.71	0.37
Point 10	0.38	1.17	0.52
Point 11	0.76	1.12	0.85
Point 12	0.77	1.33	1.20
Point 13	0.99	0.85	1.67
Point 14	1.85	1.09	2.06
Point 15	2.99	1.21	2.12
Average value	1.30	1.00	1.11
Mean square error	0.82	0.17	0.71

From the data above, the average thickness value of the copper seed layer was 1.30 μm and the mean square error was 0.82 μm. The thickest point was 2.99 μm, and the thinnest point was only 0.38 μm. The uniformity of the copper seed layer was very poor. It was easy to fail at the thinnest point. The average thickness value of the parylene layer was 1um, and the mean square error was 0.17 μm. The values measured from each measurement point were basically offset by 1 μm. The parylene layer was more uniform. The average thickness value of the silicon dioxide layer was 1.11 μm, and the mean square error was 0.71 μm. The thickness of the silicon dioxide layer decreased as the depth of the silicon via increased. The thickest point was 2.3 μm, and the thinnest point was only 0.33 μm. The uniformity of the silicon dioxide layer was poor as well.

According to the thickness data of the boundary layers in Table 1, a thickness change line chart can be generated, as shown in Figure 11.

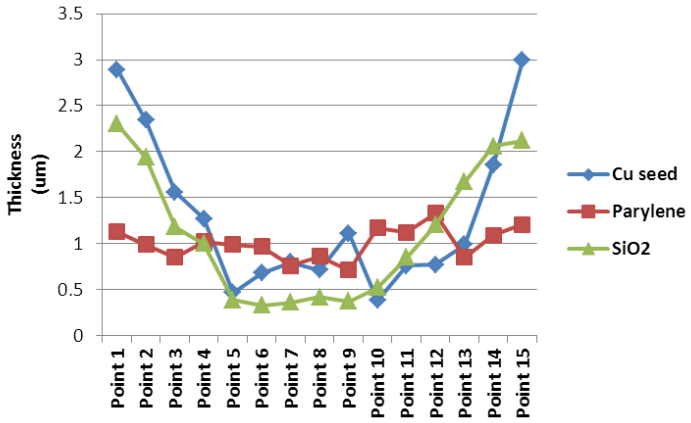


Figure 11. Thickness change line chart of boundary layers

From the above chart, the copper seed layer at the top was thicker than the bottom. The copper seed layers were made by magnetron sputtering, a physical vapor deposition (PVD) method. The copper plasma ionized by argon glow discharge was composed of charged copper ions and neutral copper ions. Neutral copper ion flow is isotropic, so it was easier to accumulate in the upper part of the silicon via. Only the charged copper ion flow, under the guidance of the current, could more easily access the deeper parts of the silicon via. There were less copper ions entering the bottom of the silicon vias, so the thickness of the copper seed layers decreased with depth.

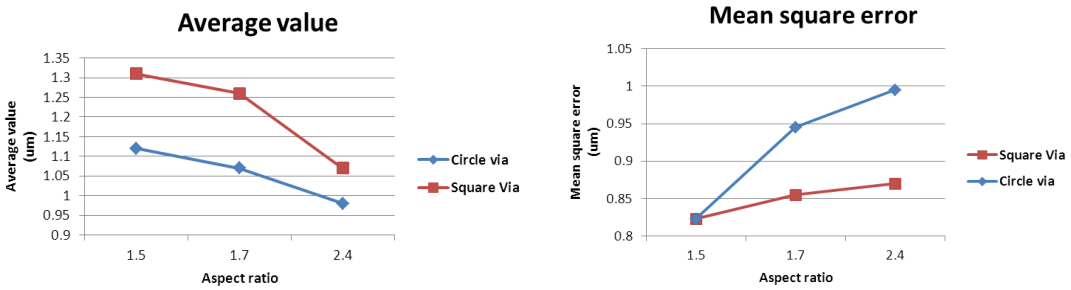
Because the copper seed layers at the top were thicker, the silicon via may have closed in advance at the top in the filling process. In other words, there would be voids at the bottom.

In terms of the above method, the thickness of the copper seed layer of the six vias S3, S5, S8, C3, C5, and C8 was measured, as shown in Table 2.

Table 2. Thickness data of the copper seed layer of different vias

Via No.	S3	S5	S8	C3	C5	C8
Diameter/Side length (μm)	79.6	71.1	48.6	78.6	67.6	46.2
Depth (μm)	120.0	122.8	115.3	115.0	115.5	111.2
Aspect ratio	1.5	1.7	2.3	1.5	1.7	2.4
Average value (μm)	1.31	1.26	1.07	1.12	1.07	0.98
Mean square error (μm)	0.823	0.855	0.870	0.823	0.945	0.995

As shown in Figure 12, the average thickness value of the copper seed layers decreased with an increasing aspect ratio. However, the mean square error of the copper seed layers increased. Therefore, the uniformity of the copper seed layers deteriorated with an increasing aspect ratio. In addition, the copper seed layers of the square silicon vias were thicker and more homogeneous than the circle silicon vias.



(a) Average value (b) Mean square error

Figure 12. Thickness change line chart of copper seed layer with aspect ratio

4.4. Boundary Layers Defect

As shown in Figure 13, the TSV boundary was divided into three layers. The first layer was the copper seed layer for electroplating copper. The second layer was the buffer layer of parylene. The third layer was the insulating layer of SiO_2.

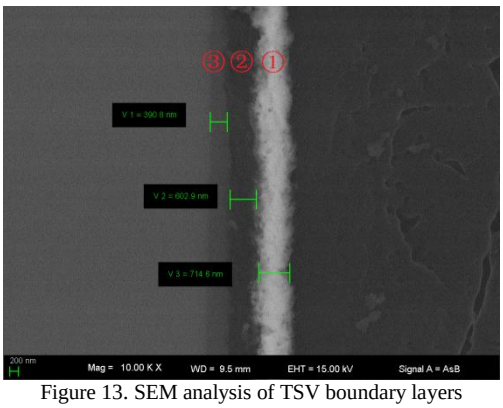
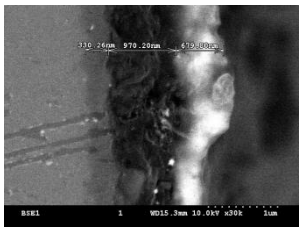
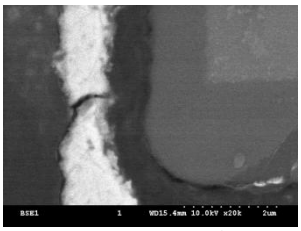


Figure 13. SEM analysis of TSV boundary layers

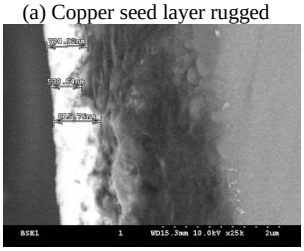
According to SEM analysis, defects of boundary layers were observed. Figure 14(a) and Figure 14(c) showed copper seed layer rugged, Figure 14(b) showed copper seed layer fracture, and Figure 14(d) showed copper seed layer missing.



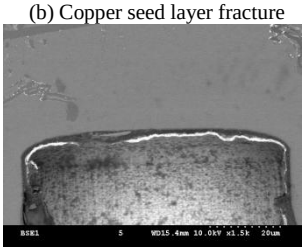
(a) Copper seed layer rugged



(b) Copper seed layer fracture



(c) Copper seed layer rugged



(d) Copper seed layer missing

Figure 14. Various defects of copper seed layer

The copper seed layer is better-proportioned and continuous, and there are fewer voids and cracks in the copper plating. That is, voids and cracks in the silicon vias are largely dependent on the flatness of the copper seed film. The roughness of the copper seed film is related to many parameters in the magnetron sputtering process, including bias voltage, silicon substrate temperature, plating time, and reaction chamber pressure.

As shown in Figure 15, if the surface of the copper seed layer is not flat and the thickness of the copper seed layer is not uniform, voids and cracks may occur at the thinnest location of the copper seed layer. This is because the copper seed layer at the thinnest location may dissolve and be lost in the electroplating process.

It was also found that the parylene layer was delaminated from the silicon dioxide layer, as shown in Figure 16 from SEM analysis. From EDS analysis, the main component of the filaments between the parylene layer and the silicon dioxide layer was parylene. It was speculated that delamination was produced by stress stretching due to the mismatch of thermal expansion coefficients of the parylene layer and the silicon dioxide layer.

From the point of view of the technical process, if the silicon dioxide layer was not cleaned before, adhesion between the parylene layer and the silicon oxide layer would be poor. In addition, certain gases introduced in the actual process production, such as HF, will have a significant effect on the adhesion of the parylene and the silicon dioxide.

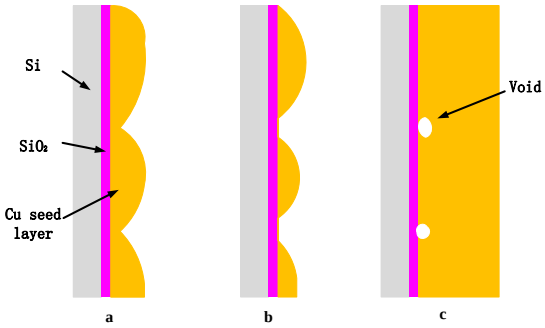


Figure 15. Void formation process: (a) uneven seed layer; (b) the seed layer partially dissolved in plating solution; (c) the void appeared at the thinnest location of the copper seed layer

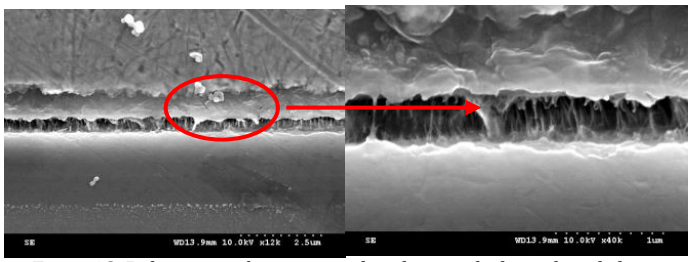


Figure 16. Delamination between parylene layer and silicon dioxide layer

5. Results and Discussion

According to a series of experimental analysis on the TSV samples, it was found that there were several process defects:

- The series of silicon vias were narrow at the top and wide at the bottom because the etching gases ratio was too large in the drilling process. These positive trapezoidal vias would cause the silicon via closing in advance at the top in next filling process, so the silicon via would not be filled completely.
- Copper seed layers were uneven. The copper seed layer at the top was thicker than that at the bottom. The uniformity of the copper seed layers deteriorated with an increasing aspect ratio. In addition, the copper seed layers of square silicon vias were thicker and more homogeneous than those of circle silicon vias.
- Fractured and missing copper seed layers were observed. Delamination between the parylene layer and the silicon dioxide layer was also observed.

According to the analysis of the production process and physical mechanism of defect formation, the following suggestions were put forward:

- In the process of deep reaction-ion etching, the proportion of the etching gas SF6 would be appropriately reduced, and the proportion of the shielding gas C4F8 would be increased.
- In the process of magnetron sputtering of copper seed film, the process parameters would be adjusted appropriately, including increasing the bias power, increasing the temperature of the silicon substrate, and setting the appropriate argon gas pressure.
- New technological means for the deposition of copper seed layer could be adopted, such as double-sided plating.
- The surface of the silicon dioxide would be cleaned before parylene deposit to improve the adhesion between the parylene layer and the silicon oxide layer

6. Conclusions

TSV three-dimensional integrated devices, which are involved in a variety of new structures, new materials, and new technology, have brought a series of new reliability issues. As an important physical connection and electrical connection between the chips, TSV's reliability is undoubtedly the key to determine the reliability of TSV three-dimensional integrated devices. The via drilling process quality and the uniformity of the boundary layers have direct and significant impacts on the performance of silicon vias.

References

1. M. G. Farooq, T. L. Graves-Abe, W. F. Landers, C. Kothandaraman, B. A. Himmel, P. S. Andry, et al., "3D Copper TSV Integration, Testing and Reliability," *in Proceedings of International Electron Devices Meeting* (*IEDM*), pp. 711-714, Washington, DC, USA, December 2011
2. T. Fukushima, Y. Yamada, H. Kikuchi, and M. Koyanagi, "New Three-Dimensional Integration Technology using Chip-to-Wafer Bonding to Achieve Ultimate Super-Chip Integration," *Japanese Journal of Applied Physics*, Vol. 45, No. 4B, pp. 3030-3035, 2006
3. I. H. Jeong, M. H. Roh, F. Jung, W. H. Song, M. Mayer, and J. P. Jung, "Analysis of the Electrical Characteristics and Structure of Cu-Filled TSV with Thermal Shock Test," *Electronic Materials Letters*, Vol. 10, No. 3, pp. 649-653, 2014
4. P. Kumar, I. Dutta, and M. S. Bakir, "Interfacial Effects During Thermal Cycling of Cu-Filled Through-Silicon Vias (TSV)," *Journal of Electronic Materials*, Vol. 41, No. 2, pp. 322-335, 2012
5. N. Ranganathan, D. Y. Lee, Y. Liu, G. Q. Lo, K. Prasad, and K. L. Pey, "Influence of Bosch Etch Process on Electrical Isolation of TSV Structures," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, Vol. 1, No. 10, pp. 1497-1507, 2011
6. R. P. Koseski, W. A. Osborn, S. J. Stranick, F. W. DelRio, M. D. Vaudin, T. Dao, et al., "Micro-Scale Measurement and Modeling of Stress in Silicon Surrounding a Tungsten-Filled Through-Silicon Via," *Journal of Applied Physics*, Vol. 110, pp. 073517, 2011
7. J. H. Lau and T. G. Yue, "Effects of TSVs (Through-Silicon Vias) on Thermal Performances of 3D IC Integration System-in-Package (SiP)," *Microelectronics Reliability*, No. 52, pp. 2660-2669, 2012
8. O. Chukwudi, W. L. June, G. Fardad, H. Klaus, and Y. S. Obeng, "A Detailed Failure Analysis Examination of the Effect of Thermal Cycling on Cu TSV Reliability," *IEEE Transactions on Electron Devices*, Vol. 61, No. 1. pp. 15-22, January 2014
9. T. Frank, S. Moreau, C. Chappaz, P. Leduc, L. Arnaud, A. Thuaire, et al., "Reliability of TSV Interconnects: Electromigration, Thermal Cycling, and Impact on above Metal Level Dielectric," *Microelectronics Reliability*, No. 53, pp. 17-29, 2013
10. E. Beyne, "The 3-D Interconnect Technology Landscape," *IEEE Design Test*, Vol. 33, No. 3, pp. 8-20, 2016
11. Y. Zhao, S. Khursheed, and B. M. Al-Hashimi, "Online Fault Tolerance Technique for TSV-Based 3-D-IC," *IEEE Transactions on Very Large Scale Integrated* (*VLSI*) *System*, Vol. 23, No. 8, pp. 1567-1571, August 2015
12. K. Croes, J. D. Messemaeker, Y. Li, W. Guo, and O. Pedreira, "Reliability Challenges Related to TSV Integration and 3-D Stacking," *IEEE Design Test*, Vol. 33, No. 3, pp. 37-45, 2015
13. J. M. Chan, C. S. T. Kheng, C. Lee, X. Cheng, and W. Kanert, "Reliability Evaluation of Copper (Cu) Through-Silicon Vias (TSV) Barrier and Dielectric Liner by Electrical Characterization and Physical Failure Analysis (PFA)," in *Proceedings of 67th Electronic Components and Technology Conference*, pp. 73-79. Florida, USA, May 30-June 2, 2017
14. P. Coudrain, P. Souare, S. Dumas, C. Chancel, and A. Farcy, "Experimental Insights into Thermal Dissipation in TSV-based 3-D Integrated Circuits," *IEEE Design Test*, Vol. 33, No. 3, pp. 21-36, 2015
15. M. J. Gaudestad, A. Orozco, I. D. Wolf, T. Wang, and T. Weber, "Failure Analysis Work Flow for Electrical Shorts in Triple Stacked 3D TSV Daisy Chains," in *Proceedings of 40th International Symposium for Testing and Failure Analysis*, pp. 38-42, Houston, USA, November 2014
16. C. C. Lee, Y. M. Lin, C. P. Hsieh, Y. Y. Liou, C. J. Zhan, T. C. Chang, et al., "Assembly Technology Development and Failure Analysis for Three-Dimensional Integrated Circuit Integration with Ultra-Thin Chip Stacking," *Microelectronic Engineering*, No. 156, pp. 24-29, 2016
17. C. Y. Liu, P. S. Kuo, C. H. Chu, A. Gu, and J. Yoon, "High Resolution 3D X-Ray Microscopy for Streamlined Failure Analysis Workflow," in *Proceedings of 23rd International Symposium on the Physical and Failure Analysis of Integrated Circuits* (*IPFA*), pp. 216-219, Singapore, July 2016
18. G. Li, Z. Chen, S. Cao, H. Luo, L. I. Jiang, and W. H. Zhu, "Failure Analysis on the Mechanical Property of Through-Silicon Vias Interface using a Cohesive Zone Model," in *Proceedings of 17th International Conference on Electronic Packaging Technology*, pp. 1341-1345, Wuhan, China, August 2016
19. M. Y. Mehr, A. Bahrami, H. Fischer, S. Gielen, and R. Corbeij, "An Overview of Scanning Acoustic Microscope, a Reliable Method for Non-Destructive Failure Analysis of Microelectronic Components," in *Proceedings of 16th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems*, pp. 1-4, Budapest, Hungary, April 2015
20. V. N. Sekhar, S. Neo, L. H. Yu, A. D. Trigg, and C. C. Kuo, "Non-Destructive Testing of a High Dense Small Dimension Through Silicon Via (TSV) Array Structures by using 3D X-Ray Computed Tomography Method (CT Scan)," in *Proceedings of 12th IEEE Electronics Packaging Technology Conference* (*EPTC*), pp. 462-466, Singapore, December 2010
21. F. X. Che, W. N. Putra, and A. Heryanto, "Study on Cu Protrusion of Through-Silicon Via," *Components, Packaging and Manufacturing Technology*, Vol. 3, No. 5, pp. 732-739, 2013
22. I. De Wolf, K. Croes, O. V. Pedreira, R. Labie, A. Redolfi, D. P. M. Van, et al., "Cu Pumping in TSVs: Effect of Pre-CMP Thermal Budget," *Microelectronics Reliability*, Vol. 51, No. 9, pp. 1856-1859, 2011
23. J. D. Messemaeker, O. V. Pedreira, B. Vandevelde, H. Philipsen, I. De-Wolf, E. Beyne, et al., "Impact of Post-Plating Anneal and Through-Silicon Via Dimensions on Cu Pumping," in *Proceedings of 63rd Electronic Components and Technology Conference*, pp. 586-591, Vegas, NV, USA , May 2013
24. L. Huang, Q. Deng, M. Li, X. Feng, and L. Gao, "A View on Annealing Behavior of Cu-Filled Through-Silicon Vias (TSV)," *ECS Journal of Solid State Science and Technology*, Vol. 5, No. 7, pp. 389-392, 2016
25. E. J. Cheng and Y. L. Shen, "Thermal Expansion Behavior of Through-Silicon-Via Structures in Three-Dimensional Microelectronic Packaging," *Microelectronics Reliability*, Vol. 52, No. 3, pp. 534-540, 2012